ABSTRACT OF THE DISCLOSURE

A multithread pipelined instruction decoder to clock, clear and stall an instruction decode pipeline of a multi-threaded machine to maximize performance and minimize power. A shadow pipeline shadows the instruction decode pipeline maintaining a the thread-identification and instruction-valid bits for each pipestage of the instruction decoder. The thread-id and valid bits are used to control the clear, clock, and stall of each pipestage of the instruction decoder. Instructions of one thread can be cleared without impacting instructions of another thread in the decode pipeline. In some cases, instructions of one thread can be stalled without impacting instructions of another thread in the decode pipeline. In the present invention, pipestages are clocked only when a valid instruction needs to advance in order to conserve power and to minimize stalling.